ABSTRACT OF THE DISCLOSURE

A transparent memory array has a processor and a plurality of memory banks, each memory bank being directly connected to the processor. The memory array has improved throughput performance in part because it can function without precharge signals, row address latch signals, and column address latch signals, among others. The transparent memory array further comprises a plurality of row address decoders, each having a row address input bus and a row address output bus. One row address decoder's input bus is connected to the processor, while its output bus is connected to a first memory bank. The memory array is also comprised of a plurality of column address decoders, each having a column address input bus and a column address output bus. One column address decoder's input bus is connected the processor, while its output bus connected to the first memory bank.